ABSTRACT OF THE DISCLOSURE

Provided is an information processing unit including: a prefetch buffer for fetching an instruction through a bus with its width being twice or more as large as an instruction length, to store the prefetched instruction; a decoder for decoding the instruction stored in the prefetch buffer; and an arithmetic unit for executing the decoded instruction. An instruction request control circuit performs a prefetch request to prefetch a branch target instruction when a branch instruction is decoded, otherwise the instruction request control circuit performs the prefetch request sequentially to prefetch the instructions. A prefetch control circuit fetches the branch target instruction to the prefetch buffer when the branch is ensured to occur by executing the branch instruction, while the prefetch control circuit ignores the branch target instruction when a branch does not occur.